UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/031,326	02/26/1998	JOSEPH J. KARNIEWICZ	303.376US1	8474

21186   7590   08/13/2003

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	30

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ___3___ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 30, 2003* _____ .

2a) ☐ This action is **FINAL.**   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-36* _____ is/are pending in the application.

    4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-36* _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Aug. 04, 2000* is: a) ☒ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some* c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    *See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____

DETAILED ACTION

This Office Action is response to RCE for application S/N: 09/031,326, filed on June 30,

2003. Claims 1-36 are pending in this official action.

Claim Objections

1.   The numbering of claims is not in accordance with 37 CFR 1.126 which requires the

original numbering of the claims to be preserved throughout the prosecution. When claims are

canceled, the remaining claims must not be renumbered. When new claims are presented, they

must be numbered consecutively beginning with the number next following the highest

numbered claims previously presented (whether entered or not).

Improperly numbered dependent claim 30 has been renumbered as claim 31.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
> in section 102 of this title, if the differences between the subject matter sought to be patented and the prior
> art are such that the subject matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be
> negatived by the manner in which the invention was made.

3.   Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madhavan et

al., US patent no. 5,675,545, in view of Ho, William, US patent no. 6,421,814 B1.

As per claims 1 and 9, Madhavan discloses method and design system for designing and

testing semiconductor memory with feature limitations substantially similar to the claimed

invention (Abstract and "Summary of the Invention"). According to Madhavan, the design

apparatus includes global files for global variables and design data relating to layout or

schematics layout and connectivity data of the functional block, a plurality of cell configuration

files or claimed local files, each relating a plurality of local variables to the global variables in

system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-

50, for example), and a plurality of cells, each cell corresponding to a local file and having a set

of parameters derived by relating the local variables to the global variables in the global source

files such that the changes of global variables in the global files reflect or may cause changes in

the programmable cells, including layout of the hierarchical semiconductor structure in

accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50).

Madhavan does not expressly disclose geometric variables related to physical layout in

hierarchical manner as claimed. Practitioner in the art at the time of the invention was made

would have found Madhavan physical semiconductor memories in the integrated circuit area

could have geometric shapes or sizes taking geometric parameter values, occupied in the chip

area such that the chip could be tested. Such geometrical feature is also well-known in the

semiconductor circuit design. In fact, Ho teaches geometrical layout variables or parameters and

such relations in geometrical layout data for physical design with faster and better layout in

integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines

33-60).

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to better improve and faster layout processing in circuit design and testing as in Madhavan.

As per claims 2-3 and 10-11, Madhavan discloses local files would obviously include inherent file from source files, instance files, data files, etc. (Figs. 9-11).

As per claim 4, Madhavan discloses master files in hierarchical design acting as initial version of a corresponding local file for design, modification, increment compilation, etc.

As per claim 5, Madhavan discloses file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Madhavan discloses file extraction and related variable extraction for design and update design.

As per claims 7-8, Madhavan discloses the design display in local host for display interactively interface.

As per claim 12, Madhavan discloses file update including update global file for coordinate process.

As per claim 13, Madhavan discloses local display in local user workstation for the design process.

As per claim 14, Madhavan discloses computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, Madhavan discloses method and design system for designing and testing

semiconductor memory with feature limitations substantially similar to the claimed invention

(Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus

includes global files for global variables and design data relating to layout or schematics layout

and connectivity data of the functional block, a plurality of cell configuration files or claimed

local files, each relating a plurality of local variables to the global variables in system files (Figs.

9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example),

and a plurality of cells, each cell corresponding to a local file and having a set of parameters

derived by relating the local variables to the global variables in the global source files such that

the changes of global variables in the global files reflect or may cause changes in the

programmable cells, including layout of the hierarchical semiconductor structure in accordance

with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does

not expressly disclose geometric variables related to physical layout in hierarchical manner as

claimed. Practitioner in the art at the time of the invention was made would have found

Madhavan physical semiconductor memories in the integrated circuit area could have geometric

shapes or sizes with geometric parameters occupied in the chip area such that the chip could be

tested. Such geometrical feature is also well-known in the semiconductor circuit design. In fact,

Ho teaches geometrical layout variables or parameters and such relations in geometrical layout

data for physical design with faster and better layout in semiconductor integrated circuit design

(Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60).

This would motivate practitioner in the art at the time of the invention was made to use

Ho teaching of geometrical layout variables in hierarchical relationships for physical design of

the integrated circuit as disclosed in Madhavan to better improve and faster physical layout

design and testing complex circuit with hierarchical structure to improve test performance.

Similarly, claims 16-21 are also rejected due to its similarities to claims 2-8 and claims

11-14.

As per claim 22, Madhavan discloses method and design system for designing and testing

semiconductor memory with feature limitations substantially similar to the claimed invention

(Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus

includes global files for global variables and design data relating to layout or schematics layout

and connectivity data of the functional block, a plurality of cell configuration files or claimed

local files, each relating a plurality of local variables to the global variables in system files (Figs.

9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example),

and a plurality of cells, each cell corresponding to a local file and having a set of parameters

derived by relating the local variables to the global variables in the global source files such that

the changes of global variables in the global files reflect or may cause changes in the

programmable cells, including layout of the hierarchical semiconductor structure in accordance

with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does

not expressly disclose geometric variables related to physical layout in hierarchical manner as

claimed. Practitioner in the art at the time of the invention was made would have found

Madhavan physical semiconductor memories in the integrated circuit area could have geometric

shapes or sizes, and the shape and size could be changed in order to fit to a fix occupied chip area

such that the chip could be design ed and tested. Such geometrical feature is also well-known in

the semiconductor circuit design. In fact, Ho teaches geometrical layout variables or parameters

and such relations in geometrical layout data for physical design with faster and better layout in

integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines

33-60).

This would motivate practitioner in the art at the time of the invention was made to use

Ho teaching of geometrical layout variables in hierarchical relationships for physical design of

the integrated circuit as disclosed in Madhavan to improve and faster layout processing in circuit

design and testing as in Madhavan.

As per claims 23-24, Madhavan discloses inherent design file, and instance file in the

design database.

As per claim 25, Madhavan disclosure would obviously imply design framework for use

in the chip design process. Such design framework could include not limited to CADENCE

functional design system as claimed.

As per claims 26, 29, and 33, Madhavan discloses method and design system for

designing and testing semiconductor memory with feature limitations substantially similar to the

claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the

design apparatus includes global files for global variables and design data relating to layout or

schematics layout and connectivity data of the functional block, a plurality of cell configuration

files or claimed local files, each relating a plurality of local variables to the global variables in

system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of programmable cells (Background of the Invention), each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed. Practitioner in the art at the time of the invention was made would have found Madhavan physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip area such that the chip could be tested. Such geometrical feature is also well-known in the semiconductor circuit design. In fact, Ho teaches geometrical layout variables or parameters and such relations in geometrical layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60).

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to better improve and faster layout processing in circuit design and testing as in Madhavan.

As per claims 27 and 28, Madhavan discloses global files and related parameters files in the semiconductor memory design. Such design parameter files could include inherent files and instance files as claimed.

As per claim 29, Madhavan and Ho disclose means for displaying design process.

As per claim 31, Madhavan discloses update design data in database spreadsheet such as in cleansheet file (col. 7, lines 1-5, for example).

As per claim 32, Madhavan discloses display means for value changes, design files, and means for allowance of user interface.

As per claims 34-36, Madhavan disclosure could include the claimed limitations in the parametric design process.

Response to Arguments

4.   Applicant's arguments filed June 30, 2003 have been fully considered but they are moot in view of a new ground of rejection.

In response to applicant's argument to the newly amended feature in the claims, the examiner has to modify the rejection to meet the amended features.

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1.   Patent no. 6,449,757 B1, issued to Karniewicz, Joseph, on Sept. 2002.

6.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Thai Phan whose telephone number is (703) 305-3812.

        Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

        Commissioner of Patents and Trademarks

        Washington, D.C. 20231

or faxed to:

        (703) 746-7239, (for formal communications intended for entry)

Or:

        (703) 746-7240 (for informal or draft communications, please label

"PROPOSED" or "DRAFT")

        Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington. VA., Sixth Floor (Receptionist).

August 11, 2003

Thaiphan
Patent Examiner
Thai Pham
AU 2123